

PATENT

Attorney Docket No.: 728-208 (YOR9-2001-0270 US)

**AMENDMENTS TO THE CLAIMS**

1-11. (Canceled)

12. (Currently Amended) An array of planar T-RAM cells comprising:  
a plurality of T-RAM cells, said plurality of T-RAM cells being arranged in an array and  
fabricated over a substrate, each of said plurality of T-RAM cells including a buried vertical  
thyristor and a horizontally stacked pseudo-TFT transfer gate having a body of a majority portion  
of single crystalline material using an n+ layer below it as seed material by a epitaxial lateral  
overgrowth technique, said horizontally stacked pseudo-TFT transfer gate including a  
source/drain and body, said thyristor being buried underneath said horizontally stacked pseudo-  
TFT transfer gate, wherein said horizontally stacked pseudo-TFT transfer gate covers at least a  
portion ~~the entire top surface~~ of said thyristor, and further wherein the top surface of said  
horizontally stacked pseudo-TFT transfer gate forms a co-planar top surface of each said  
horizontally stacked pseudo-TFT transfer gate of each said T-RAM cell,  
wherein each of the plurality of T-RAM cells has a size of less than or equal to  $6F^2$ .

13-14. (Cancelled)

15. (Previously Presented) The array according to Claim 12, wherein said substrate is a  
semiconductor SOI or bulk wafer.

16. (Previously Presented) The array according to Claim ~~13~~<sup>12</sup>, wherein a base of said  
thyristor is surrounded by a surrounded gate.

17. (Previously Presented) The array according to Claim 12, wherein said planar top  
surface of each T-RAM cell provides for fabrication of wordlines, said wordlines being  
fabricated over said planar top surface of said T-RAM cells, said wordlines for interconnecting  
said T-RAM cells.

18-31. (Canceled)